Workshop on "Time and Dependability"

Coordinators: Paulo Veríssimo (University of Lisboa, Portugal)
Neeraj Suri (Chalmers University, Götenburg, Sweden)

First day of Workshop (Saturday, January 22)

Time-related Models, Service and Validation

Session 1 — Moderator: Paulo Veríssimo (University of Lisboa, Portugal)

Gérard Le Lannn (INRIA, Rocquencourt, France)
Time-based Models and Timing Failures

Sam Toueg (Ecole Polytechnique, Palaiseau, France)
On the Quality of Service of Failure Detectors

Session 2 — Moderator: Rick Schlichting (University of Arizona, Tucson, AZ, USA)

Ulrich Schmid (Vienna University of Technology, Austria)
High-Accuracy Time Services and Fault-Tolerant Clock Synchronization

Takashi Nanya (University of Tokyo, Japan)
An Asynchronous Superscalar Microprocessor Design

Session 3 — Moderator: Jean-Claude Laprie (LAAS-CNRS, Toulouse, France)

Hermann Kopetz (Vienna University of Technology, Austria)
Time-Triggered Architecture

Joseph Sifakis (VERIMAG, Gières, France)
Modeling of Real-Time Systems

Second day of Workshop (Sunday, January 23)

Applications: Operating Systems, Databases, Embedded Systems and Middleware

Session 4 — Moderator: Alain Costes (LAAS-CNRS, Toulouse, France)

Michael B. Jones (Microsoft Research, Redmond, WA, USA)
Predictable Execution: Operating Systems Issues

Rajeev Rastogi (Bell Labs/Lucent Technologies, Murray Hill, NJ, USA)
DataBlitz – Main Memory DataBase System

Session 5 — Moderator: Jay Lala (DARPA, Arlington, VA, USA)

David Powell (LAAS-CNRS, Toulouse, France)
Using Communication by Time to Implement Fail-Safe Duplex Redundancy

Gordon S. Blair (University of Lancaster, UK)
Quality of Service Middleware

Session 6 — Moderator: Neeraj Suri (Chalmers University of Technology, Götenburg, Sweden)

Workshop Wrap up
Walter Heimerdinger (Honeywell Technology Center, Minneapolis, MN, USA)